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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,554	09/15/2003	Hiep The Pham	P214/WLP	3559
25670	7590	12/01/2004	EXAMINER	
WILLIAM L. PARADICE, III 2686 MCALLISTER STREET SUITE 1 SAN FRANCISCO, CA 94118				NGUYEN, HAI L
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/662,554	PHAM, HIEP THE
Examiner	Art Unit	
Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 15 September 2003.

2a)  This action is **FINAL**.                            2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## **Disposition of Claims**

4)  Claim(s) 1-39 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1,2,13-34 is/are rejected.

7)  Claim(s) 3-12 and 35-39 is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 15 September 2003 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date .

4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .

5)  Notice of Informal Patent Application (PTO-152)

6)  Other: \_\_\_\_\_

**DETAILED ACTION**

*Specification*

1. The disclosure is objected to because of the following informalities: page 14, line 29; “GS” should be changed to --GC—as shown in Fig. 6.

Appropriate correction is required.

*Claim Rejections - 35 USC § 112*

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 21-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In claim 8, the recited limitation “a controller for generating the tuning range control signal and the reset signal in response to a plurality of reference voltages and a mode signal”, on the last 3 lines, is not enabled by the present specification because with such limited limitations, as recited above, it is not understood how the instant invention can perform the claimed function “generating the tuning range control signal”.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 13-19 and 21-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 13 is indefinite because of the recited limitation “a finite state machine having first inputs to receive the compare signals, and first outputs to generate the one or more tuning range control signals in response to the compare signals” on the last 3 lines. It is misdescriptive because the finite state machine (604 in instant Fig. 6) does not generate the one or more tuning range control signals (TRS) to the VCO (340 in instant Fig. 3) as recited in the claim, but rather generates the shift signals (SH\_up, SH\_dn) to the counter (606).

Claims 14-17 are rendered indefinite by the deficiencies of base claim 13.

7. Claim 18 is indefinite because of the recited limitation “a multiplexer having a first input to receive the counter signal, a second input to receive the one or more mode signals, a control terminal to receive a logic combination of the one or more mode signals, and an output to provide the tuning range signals to the VCO” on the last 5 lines. It is misdescriptive because the multiplexer (608 in instant Fig. 6) does not generate the tuning range signals (TRS) to the VCO (340 in instant Fig. 3) as recited in the claim, but rather generates the control signals (GC) to the decoder (612).

Claim 19 is rendered indefinite by the deficiencies of base claim 18.

8. Claims 21-33 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted element is: the control voltage (V\_ctrl in instant Fig.3) as input

signal to the controller (350). In order for the controller for generating the tuning range control signal (TRS), the omitted element needs to be included in the claims.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2, 20, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Nise (US 5,696,468).

With regard to claims 1 and 34, Nise discloses in Figs. 1-5 a phase-locked loop (PLL) circuit, and a method of use thereof, comprising a phase detector (12); a charge pump (see column 8, lines 19-41); a loop filter (VM, SW1, 20, C) having an input to receive the control voltage (VC) and having a control terminal (P7, P8); a voltage-controlled oscillator (16); and a controller (22-38, 10, 14) having inputs to receive the control voltage, a high reference voltage (VH), a low reference voltage (VL), and one or more mode signals (36, 38), and having a first output (P3, P4) connected to the control terminal of the loop filter and second outputs (IV, Ioffset) to generate the tuning range signals.

With regard to claims 2 and 20, the references also meet the recited limitations in these claims.

***Allowable Subject Matter***

11. Claims 3-12 and 35-39 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a specific structural limitations, as recited in claim 3, such as a controller (350 in instant Fig. 3) having inputs to receive the control voltage (V\_ctrl), a high reference voltage (VH), a low reference voltage (VL), and one or more mode signals (MS), and having a first output (RST) connected to the control terminal of the loop filter (330) and second outputs (TRS) to generate the tuning range signals, wherein the mode signals are set to a first state (00 in instant Table 2) to allow the controller to automatically generate the one or more tuning range signals; and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a specific structural limitations, as recited in claim 9, such as a differential oscillator circuit (900 in instant Fig. 9) comprises a first transistor (901) coupled between a first output terminal (OUT) and a bias node, and having a gate coupled to a second output terminal (/OUT); a second transistor (902) coupled between the second output terminal and the bias node, and having a gate coupled to the first output terminal; and a resonant circuit coupled between the first and second output terminals, and having an offset capacitor (Coffset) coupled between the first and second output terminals; a first capacitor (C0) and a first switch (SW0) connected in series between the first and second output terminals, the first switch controlled by a first tuning range control signal (TRS[0]); a second capacitor (C1) and a second switch (SW1) connected in series between the first and second output terminals, the

second switch controlled by a second tuning range control signal (TRS[1]); and a varactor (C2) coupled between the first and second output terminals, the varactor including a terminal to receive the control voltage (V\_ctrl); and being configured in combination with the rest of the limitations of the base claims and any intervening claims.

The prior art of record fails to disclose or fairly suggest a specific step, as recited in claim 35, such as selecting a lower frequency tuning range if the control voltage is less than the first reference voltage (CMP\_dn in instant Fig. 6); selecting a higher frequency tuning range if the control voltage is greater than the second reference voltage (CMP\_up); and locking the selected frequency tuning range if the control voltage is between the first and second reference voltages; and being configured in a method of operating a phase-locked loop circuit having a plurality of substantially adjacent frequency tuning ranges.

The prior art of record fails to disclose or fairly suggest a specific step, as recited in claim 38, such as asserting a shift-up signal (SH\_up in instant Fig. 6); if the control voltage (V\_ctrl) is less than the first reference voltage; asserting a shift-down signal (SH\_dn) if the control voltage is greater than the second reference voltage; incrementing a counter value (CNT) in response to the shift-up and shift-down signals; generating a tuning range control signal (TRS) in response to the counter value; and adjusting the frequency tuning range in response to the tuning range control signal.

***Conclusion***

12. Regarding claims 13-19, the patentability thereof cannot be determined because of their indefiniteness.
13. Regarding claims 21-33, the patentability thereof cannot be determined because of failing to comply with the enablement requirement and being indefiniteness.
14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Asano (US Pat. 6,667,640) is cited as of interest because it discloses a phase locked loop circuit having a wide oscillation frequency range for reducing jitter.
15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN   
November 16, 2004



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